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STEPHEN A GRATTON
2764 SOUTH BRAUN WAY
LAKEWOOD CO 80228

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Please find below and/or attached an Office communication concerning this application or proceeding.

Commissioner of Patents and Trademarks

Office Action Summary	Application No.	Applicant(s)	
	09/302,576	HEMBREE ET AL.	
	Examiner	Art Unit	
	Trung Q Nguyen	2858	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136 (a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 April 1999* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *34-51 and 68-77* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *34-51 and 68-77* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claims _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are objected to by the Examiner.

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. § 119

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. § 119(e).

Attachment(s)

15)☒ Notice of References Cited (PTO-892)
16)☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
17)☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *2 and 4* .
18)☐ Interview Summary (PTO-413) Paper No(s). _____ .
19)☐ Notice of Informal Patent Application (PTO-152)
20)☐ Other: .

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 34-37 are rejected under 35 U.S.C. 102(b) as being anticipated by Akram (741).

3. Regarding claim 34, Akram (741) discloses a method for fabricating an interconnect for a semiconductor die (abstract), comprising: providing a substrate (12) (Figure 1, column 4, line 63); forming a contact member comprising a raised portion (65, Figure 7) of the substrate at least partially covered with a conductive layer and configured to electrically contact a contact location on the die (see column 6, lines 6-25, especially lines 9-11); attaching a metal conductor to the substrate proximate to the contact member; and forming a conductive material on the substrate in electrical communication with the conductive layer and the conductor (column 3, lines 8-31, especially lines 12-17, column 11, lines 24-25).

4. Regarding claim 35, Akram (741) discloses the metal conductor comprises a copper foil laminated to a polymer film (column 7, line 37, and lines 42-54).

5. Regarding claim 36, Akram (741) discloses the conductive material comprises a conductive adhesive (column 1, line 31).

6. Regarding claim 37, Akram (741) discloses the conductive material comprises a solder (column 8, lines 34-44, especially line 37).

7. Claims 38-40 are rejected under 35 U.S.C. 102(b) as being anticipated by Wood (179).

8. Regarding claim 38, Wood (179) discloses a method for fabricating an interconnect for a semiconductor die (abstract), comprising: providing a substrate (abstract); forming a plurality of contact members on the substrate configured to electrically contact a plurality of contact locations of the die (abstract); providing a tape (column 8, lines 6-8) comprising a polymer film (column 8, line 26) and a plurality of conductors on the film including a plurality of openings (92) configured for placement on the contact; attaching the tape to the substrate with the contact members projecting through the openings (column 8, lines 16-27); and depositing a conductive material in the openings in electrical communication with the contact members and conductors members (Figure 8, column 8, lines 5-19, especially lines 6 and 13).

9. Regarding claim 40, Wood (179) discloses the conductive material comprises a conductive adhesive (column 3, lines 63-64, column 8, line 26).

Claim Rejections - 35 USC § 103

10. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

11. Claim 39 is rejected under 35 U.S.C. 103(a) as being unpatentable over Wood (179) in view of Akram (779).

Regarding claim 39, Wood (179) disclose all elements that are in claim 38, which claim 39 is depending on. Wood (179) does not disclose forming the contact members comprises etching the substrate to form pillars and then depositing conductive layers on the pillars.

Akram (779) discloses forming the contact members comprises etching the substrate to form pillars and then depositing conductive layers on the pillars (column 3, line 5).

Therefore, at the time of the subject invention, it would have been obvious for a person of ordinary skill in the art to have utilized the method and apparatus that Wood (179) and Akram (779) discloses to accomplish the design in claim 39.

The suggestion/motivation for doing so would have been that, the use of etching a substrate to a form of a pillar as describe in claim 39 is well known within the semiconductor industry.

12. Claims 41-42 are rejected under 35 U.S.C. 103(a) as being unpatentable over Wood (179) in view of Akram (741).

13. Regarding claim 41, Wood (179) disclose all elements that are in claim 38, which claim 41 is depending on. Wood (179) does not disclose the conductive material comprises a solder.

Akram (741) discloses the conductive material comprises a solder (column 8, lines 36-37).

Therefore, at the time of the subject invention, it would have been obvious for a person of ordinary skill in the art to have utilized the method and apparatus Wood (179) and Akram (741) discloses to accomplish the design in claim 41.

The suggestion/motivation for doing so would have been that, the use of a solder in a conductive material as describe in claim 41 is well known within the semiconductor industry.

14. Regarding claim 42, Wood (179) discloses the conductors comprise metal foil laminated to the polymer film (column 8, lines 16-28, especially lines, 26).

15. Claims 43-47 are rejected under 35 U.S.C. 102(b) as being anticipated by Akram (741) in view of Akram (779), Hembree and Wood (179).

16. Regarding claim 43, Akram (741) discloses a method for forming an interconnect for a semiconductor die (abstract), comprising: providing a substrate (abstract); forming a contact member on the substrate comprising a base (60)(column 5, line 59).

Akram (741) does not disclose a pillar and a projection configured to penetrate a contact location of the die to a limited penetration depth.

Akram (779) disclose a pillar and a projection configured to penetrate a contact location of the die to a limited penetration depth (column 3 lines 9-14).

Hembree discloses providing a multi layered tape comprising a polymer film and a metal conductor formed thereon (column 4, line 31); attaching the tape to the substrate with the conductor proximate to the contact member (column 10, lines 35-41).

Wood (179) discloses and electrically connecting the contact member to the conductor by depositing a conductive material on the contact member and conductor (column 10, lines 10-14).

Therefore, at the time of the subject invention, it would have been obvious for a person of ordinary skill in the art to have utilized the method and apparatus Akram (741), Akram (779), Hembree and Wood (179) disclose to accomplish the design in claim 43.

The suggestion/motivation for doing so would have been that, electrical connections are made by wire bond or tape to external pin leads adapted for plugging into sockets on a circuit board. However, with multi-chip module construction, non-encapsulated chips or dies are secured to a substrate, typically using adhesive, and have outwardly exposed bonding pads.

17. Regarding claim 44, Wood (179) discloses the conductor includes an opening aligned with the contact member and the conductive material is deposited in the opening (column 10, lines 10-14).

18. Regarding claim 45, Wood (179) discloses the conductive material comprises a conductive adhesive (column 9, lines 22-27).

19. Regarding claim 46, Akram (741) discloses the conductive material comprises a solder (column 8, lines 34-44, especially line 37).

20. Regarding claim 47, Akram (741) discloses attaching the tape comprises forming an adhesive layer between the tape and substrate (column 1, line 31).

21. Claims 48-51 are rejected under 35 U.S.C. 102(b) as being anticipated by Akram (741) in view of Kucharek and Wood (179).

22. Regarding claim 48, Akram (741) discloses a method for fabricating an interconnect for a semiconductor die (abstract), comprising: providing a substrate (abstract).

Akram (741) does not disclose forming a depression in the substrate sized to retain a bumped contact location on the die.

Kucharek discloses forming a depression in the substrate sized to retain a bumped contact location on the die covering at least a portion of the depression with conductive layer (column 17, lines 66-68, column 18, lines 1-6);

Wood (179) discloses attaching a conductor to the substrate in electrical communication with the conductive layer and electrically insulated from the substrate (column 6, lines 15-25, especially lines 23-24).

Therefore, at the time of the subject invention, it would have been obvious for a person of ordinary skill in the art to have utilized the method and apparatus Akram (741), Kucharek and Wood (179) discloses to accomplish the design in claim 48.

The suggestion/motivation for doing so would have been that, during burn-in test, a die is heated to an elevated temperature. This causes thermal expansion of the die and test fixture, stress may develop between the interconnect structure and adversely effect the electrical connection there between.

23. Regarding claim 49, Wood (179) discloses the conductor includes an opening surrounding the depression (column 10, lines 10-14).

24. Regarding claim 50, Wood (179) discloses the conductor comprises a metal foil laminated to a polymer film (column 8, lines 16-28, especially lines, 26).

25. Regarding claim 51, Wood (179) discloses attaching the conductor comprises forming an adhesive layer between the conductor and substrate (column 9, lines 22-27).

26. Claims 68-70 are rejected under 35 U.S.C. 102(b) as being anticipated by Akram (741) in view of Wood (179) and Farnworth (428).

27. Regarding claim 68, Akram (741) discloses a method for fabricating an interconnect for a semiconductor die (abstract), comprising: providing a substrate (abstract); forming a plurality of contact members on the substrate comprising conductive layers configured to electrically contact a plurality of contact location on the die (Figure 15, column 4, lines 46-49); providing a polymer film with a plurality of conductors thereon, the conductors including a plurality of openings configured for placement on the contact members (column 7, line 37, and lines 42-54).

Wood (179) discloses attaching the tape to the substrate with the openings substantially enclosing the contact (column 8, lines 6-8, column 8, line 26).

Farnworth (428) discloses depositing a conductive material in the openings in electrical communication with the conductive layers and conductors (column 6, lines 1-16, especially lines 9-11).

Therefore, at the time of the subject invention, it would have been obvious for a person of ordinary skill in the art to have utilized the method and apparatus Akram (741), Wood (179) and Farnworth (428) discloses to accomplish the design in claim 68.

The suggestion/motivation for doing so would have been that, the method for fabricating an interconnect for a semiconductor die as describe in claim 68 is inexpensive and pervasive within the semiconductor industry.

28. Regarding claims 69-70, Farnworth (428) discloses the contact members comprise raised portions of the substrate at least partially covered with the conductive layers, and the contact members comprise depressions in the substrate at least partially covered with the conductive layers (column 3, lines 4-15, especially lines 7, 11-15).

29. Claims 71-73 are rejected under 35 U.S.C. 103(a) as being unpatentable over Akram (741) in view of Akram (779) and Wood (179).

30. Regarding claim 71, Akram (741) discloses a system for testing a semiconductor die comprising: a temporary package for the die (abstract); and an interconnect on the package for establishing temporary electrical communication with the die (abstract); the interconnect comprising: a substrate (abstract).

Akram (741) does not disclose a conductive layer formed thereon configured to electrically contact a contact location on the die.

Akram (779) discloses a conductive layer formed thereon configured to electrically contact a contact location on the die (column 3 lines 9-14); and a contact member comprising a pillar formed integrally with the substrate (column 3, line 5).

Wood (179) discloses a multi layered tape bonded to the substrate comprising a polymer film and a conductor on the polymer film (column 8, lines 16-27); and a conductive material in electrical communication with the conductive layer and the conductor (Figure 8, column 8, lines 5-19, especially lines 6 and 13).

Therefore, at the time of the subject invention, it would have been obvious for a person of ordinary skill in the art to have utilized the method and apparatus that Akram (741), Akram (779) and Wood (179) discloses to accomplish the design in claim 71.

The suggestion/motivation for doing so would have been that, the type of interconnect as describe by the applicant can include electrical or structural defects which can cause the die test procedure to be affected or invalidated because an insulating layer that insulates the conductors of the interconnect from the substrate can allow current leak from one or more conductors into the substrate or the substrate can also include cracks that propagate through the insulating layer creating undesirable electrical paths in the assembled temporary package.

31. Regarding claim 72, Wood (179) discloses the conductor comprises a metal foil laminated to the polymer film (column 8, lines 16-28, especially lines, 26).

32. Regarding claim 73, Akram (471) discloses the conductive material comprises a conductive adhesive or a solder (column 8, lines 36-37).

33. Claim 74 is rejected under 35 U.S.C. 103(a) as being unpatentable over Akram (741) in view of Kucharek, Fanrworth (428) and Wood (179).

Regarding claim 74, Akram (741) discloses a system for testing a semiconductor die comprising: a temporary package for the die (abstract); and an interconnect on the package for establishing temporary electrical communication with the die (abstract); the

interconnect comprising: a substrate (abstract); and a conductive material on the substrate electrically connecting the conductive layer and the conductor (claim 1).

Akram (741) does not disclose a depression in the substrate configured to retain a bumped contact location on the die; a conductive layer at least partially covering the depression.

Kucharek discloses a depression in the substrate configured to retain a bumped contact location on the die (column 17, lines 66-68, column 18, lines 1-6);

Fanrworth (428) discloses a conductive layer at least partially covering the depression (column 3, lines 4-15, especially lines 7, 11-15);

Wood (179) discloses a tape attached to the substrate comprising a polymer film and a conductor on the polymer film with an opening proximate to the depression (column 8, lines 16-27).

34. Therefore, at the time of the subject invention, it would have been obvious for a person of ordinary skill in the art to have utilized the method and apparatus of Akram (741), Kucharek, Fanrworth (428) and Wood (179) discloses to accomplish the design in claim 74.

The suggestion/motivation for doing so would have been that, temporary electrical connection is desirable to effect a connection that causes as little damage as possible to the bond pad. If the temporary connection to a bond pad damages the pad, the entire die may be rendered as unusable.

35. Claims 75-77 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tuttle in view of Liu and Hembree.

36. Regarding claim 75, Tuttle discloses a system for testing semiconductor dice contained on a wafer (column 3, line 13), comprising: a wafer probe handler in electrical communication with testing circuitry (column 8, lines 14-17).

Tuttle does not disclose a probe card mounted to the wafer probe handler comprising a substrate and a plurality of contact members configured to electrically connect to contact locations on the dice.

Liu discloses a probe card (8) mounted to the wafer probe handler comprising a substrate and a plurality of contact members configured to electrically connect to contact locations on the dice (abstract, column 6, lines 57-63).

Hembree discloses a tape comprising a polymer film and a plurality of conductor in electrical communication with the contact members (column 4, line 31); the tape configured to physically attach the probe card to the wafer probe handler with the contact members in electrical communication with the testing circuitry (column 10, lines 35-41).

Therefore, at the time of the subject invention, it would have been obvious for a person of ordinary skill in the art to have utilized the method and apparatus that Tuttle, Liu and Hembree discloses to accomplish the design in claim 75.

The suggestion/motivation for doing so would have been that, the use tape for physically attach the probe card to the wafer probe handler with the contact members in

electrical communication with the testing circuitry as describe in claim 75 is inexpensive and pervasive within the semiconductor industry.

37. Regarding claim 76, Wood (179) discloses a conductive adhesive for electrically connecting the contact members to the conductors (column 9, lines 22-27).

38. Regarding claim 77, Tuttle discloses a solder for electrically connecting the contact members to the conductors (column 8, lines 14-16 and 33).

Conclusion

39. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

As already mentioned, there are a number of prior art references dealing with the use of hybrid interconnect and system for testing semiconductor dice; only a representative sample is cited herein.

Akram (807) discloses (abstract) A method is disclosed of forming a high elevation area and a low elevation area in a substrate and of electrically interconnecting the high elevation area and the low elevation area. The method includes anisotropically etching into a non-masked portion of monocrystalline silicon in a selective manner of one silicon plane relative to another silicon plane to produce a high elevation area and a low elevation area which are laterally angled relative to one

another. The high elevation area and the low elevation area thereby interconnected by a substantially planar, non-perpendicularly angled surface. Such areas and plane are then doped to form a continuous electrically conductive and interconnecting diffusion region extending from the high elevation area, through and along the angled surface to the low elevation area. A semiconductor apparatus having the above construction is also disclosed. Also disclosed is an epitaxial silicon growth and etching process, and a semiconductor apparatus having multiple different monocrystalline silicon portions. Further disclosed is a method of producing a testing apparatus having a projection formed essentially of electrically conductive polysilicon.

Leedy discloses (see Figures 5-7, abstract) Each transistor or logic unit on an integrated circuit wafer is tested prior to interconnect metallization. By CAD means, the transistor or logic units placement net list is revised to substitute redundant defect-free logic units for defective ones. Then the interconnect metallization is laid down and patterned under control of a CAD means. Each die in the wafer thus has its own interconnect scheme, although each die is functionally equivalent, and yields are much higher than with conventional testing at the completed circuit level. The individual transistor or logic unit testing is accomplished by a specially fabricated flexible tester surface made in one embodiment of several layers of flexible silicon dioxide, each layer containing bias and conductive traces leading to thousands of microscopic metal probe points on one side of the test surface. The probe points electrically contact the contacts on the wafer under test by fluid pressure. The tester surfaces traces are then connected, by means of multiplexers, to a conventional tester signal processor.

Wojnarowski discloses (see Figure 4, abstract) In fabricating wafer scale integrated interconnects, a temporary or permanent dielectric layer and a pattern of electrical conductors are used to provide wafer scale integration or testing and burn-in. A resist can be used to cover the areas of IC pads on the wafer while the remainder of the pattern of electrical conductors is removed to provide for repair of the wafer scale integration structure. The pattern of electrical conductors may be configured so that the conductor lengths between at least some sub-circuits on a plurality of wafers are substantially electrically equal for signal propagation purposes; an additional wafer may be laminated to the wafer using an adhesive; controlled curfs may be cut into the wafer; and the wafer may be interconnected to an interface ring.

40. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Trung Nguyen whose telephone number is 703-305-4925. The examiner can normally be reached on Monday through Friday, 8:30AM – 5:00PM. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Safet Methajic can be reached on 703-308-1436.

TN

May 24, 2001

Safet Metjahic
Supervisory Patent Examiner
Technology Center 2800